Int. J. Advance. Soft Comput. Appl., Vol. 6, No. 3, November 2014
ISSN 2074-8523

Development of Multi-Standard Digital Radio Chipset with Shared Logic and Memory

Se-Ho Park[1], Jeongwook Seo[2], and Min-Goo Kang[3]

[1]Contents Convergence Research Center, Korea Electronics Technology Institute
[2]Department of Information & Communication Eng., Namseoul University
[3]Division of Information & Telecommunications, Hanshin University
e-mail: kangmg@hs.ac.kr (Corresponding Author)

Abstract

The digital transition of analog TV is rapidly taking place throughout the world. However, the digital transition of radio is progressing at a slower rate. Diverse standards are being considered for adoption and different countries have different frequencies allocated for digital radio. As a consequence, the progress in the development of digital radio receiver chipsets has been rather stagnant. In this paper, the design and implementation of a receiver chipset with integrated baseband and RF tuner block is presented for DAB/DAB+, DRM30/DRM+, and HD Radio digital radio standards. The developed chipset can receive broadcast from all standards and frequencies considered through simple software change.

Keywords: *Digital Audio Broadcasting, Digial Radio Mondiale, Digital Radio chipset, HD Radio, Multi-Standard Receiver.*

1 Introduction

In order to improve the audio quality of existing AM/FM radio various digital radio standards have been developed. Currently, many countries are in the process of digitalizing the analog radio by adopting a digital radio standard which conforms to the local frequency and broadcasting policies [1],[2]. Each country is selecting its own digital radio standard and the digital transition period is different among countries. These events have led to the delay in the development of digital radio receiver chipsets. In this paper, we introduce the design and implementation of a baseband demodulator chip and RF receiver chip that

can receive and process Digital Radio Mondiale (DRM/DRM+), Digital Audio Broadcasting (DAB/DAB+), and HD Radio broadcasts. DRM/DRM+, DAB/DAB+, and HD Radio are digital radio standards that are most widely adopted throughout the world. The integrated digital radio receiver chipset design proposed can receive high-quality audio and diverse data services offered by the different broadcasting standards in a single, integrated chipset. In addition, the diverse hardware blocks that are used to enable reception in the mobile environment have been designed to be shared among the different standards, in order to decrease the overall chip size and reduce power consumption.

2 Review of Digital Radio Standards

Digital radio broadcasting offers high-quality audio and diverse data services compared to existing analog broadcasting. Universal adoption of a single digital radio standard is not possible, since each country has different frequency regulations and policies for digital radio transition. Therefore, diverse digital radio standards are being adopted throughout the world. The frequency bands used varies from a few kilohertz to several gigahertz which makes receiver chipset implementation a challenge. In this section, the requirements for each of the digital radio standards are analyzed, in order to design a receiver chipset that conforms to all digital standards.

2.1 Digital Audio Broadcasting

Eureka-147 (European research coordination agency project-147) is the name of the next-generation digital radio project that started in Europe, led by the United Kingdom. During its commercialization phase the name Digital Audio Broadcasting (DAB) was given [3],[4]. ETSI, which is Europe's telecommunications standardization body, selected DAB as the European standard (ETSI EN300 401) in 1995. Following, ITU-R selected DAB as System A in the BO.1130-4 recommendation. The DAB standard has further evolved into DAB+ and T-DMB Audio, expanding the scope of the standard. DAB, DAB+, and T-DMB Audio are DAB family of standards. They are almost identical with the exception of the use of the audio codec. DAB is robust against noise and multipath interference compared to analog AM/FM broadcasting and provides CD quality sound. DAB+ offers twice the transmission capacity of DAB. Each multiplex can transmit 24 programs (48 kbit/s for each program) using DAB+. The carrier frequency used in the DAB standard varies from a few megahertz to 1.5 GHz depending on the mode of operation, and its bandwidth is 2.048 MHz. Most countries use mode 1 with carrier frequency bands of below 375 MHz [4].

Table 1: Characteristics of digital radio standards

Parameters	DAB/DAB+	DRM/DRM+	HD Radio
Frequency Band	Band-I, II, III IV, L-Band	< 30MHz(DRM) < 174MHz(DRM+)	AM: MF FM: 88-108MHz
Bandwidth (kHz)	1536	4.5/5/9/10/18/20 96(DRM+)	AM: 30(H),20(A) FM: 140(H),400(A)
Tansmission	OFDM	OFDM	OFDM
Modulation	π/4DQPSK	4/16/64QAM	AM: 2/4/16/64QAM FM: QPSK
Channel Coding	PCC R=1/4,3/8,1/2,3/4	PCC-based MLC RS+CC for Packet	CPPCC
Data Rate (kbps)	1152(PL3)	20-24(9 10kHz) 35-190(100kHz)	AM: 36(AU),1.2(DA) FM: 96(AU),48(DA)
Audio Codec	MUSICAM HE-AAC v2	AAC/CELP/HXVR+SBR MPS 5.1/7.1	HDC

2.2 Digital Radio Mondiale

DRM (Digital Radio Mondiale) was developed by a joint consortium of American and European companies. In the second half of 2009, ETSI approved DRM as a new digital radio standard (ETSI ES 201 980 v3.1.1) in [5]. DRM is a digital radio standard that uses transmission bandwidths of 9 kHz or 10 kHz and uses MPEG-4 AAC with Spectral Band Replication (SBR) as the audio codec. DRM was initially developed as a digital solution for AM frequencies of below 30 MHz (DRM30) [6]. Due to technical improvements, the original DRM standard has been expanded to cover frequencies between 150 kHz to 120 MHz (DRM+). As radio broadcasters are allowing higher bitrates in the FM band, DRM+ supports data rates of 190 kbit/s using 100 kHz of bandwidth, in order to provide high-quality CD-like audio [5].

2.3 HD Radio

HD Radio was developed by Ibiquity, a company based in North America. HD Radio is based on a radio technology known as In-Band On-Channel (IBOC) [7],[8]. HD Radio is a digital radio standard that replaces FM bands between 88 and 108 MHz and AM bands between 525 and 1705 kHz. HD Radio was designed to provide a smooth digital transition from analog radio. It supports a hybrid mode of broadcasting in which both analog FM and digital broadcasting can be serviced simultaneously. HD Radio also supports full digital mode which transmits digital-only broadcasting in the AM and FM bands. Until 2003, HD Radio used the PAC audio codec. Beginning 2003, it has been employing High-Definition Coding (HDC) codec which is similar to MPEG-4 HE-AAC. Under hybrid mode transmission, a maximum of 151 kbit/s data throughput

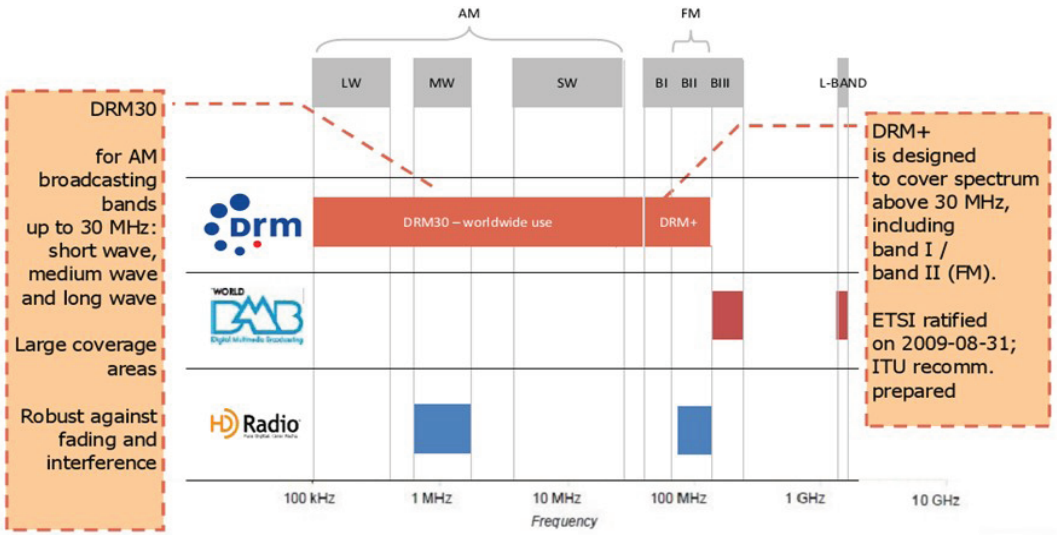

Figure 1: Frequency bands in digital radio standards.

with a maximum of 140 kHz bandwidth is supported. In full digital mode transmission, a maximum of 300 kbit/s data throughput with a maximum of 400 kHz bandwidth is supported.

2.4 Comparison of Digital Radio Standards

Table 1 summarizes the characteristics of each of the digital radio broadcasting standards. All of the standardized digital radio broadcasting technologies use OFDM transmission method and share similarities in many aspects such as channel coding and audio codec. Such similarities allow the use of a common sub-block when designing the baseband demodulator. The sub-block implemented is not used for the decoding of a particular digital radio standard signal. It is used for the decoding of all digital radio standards signals thereby increasing the logic reuse and decreasing the implementation logic size. In addition to the Baseband Decoder Core block, other blocks such as ADC, digital filtering, audio codec, and data stream decoder have also been designed with logic reuse in mind. The frequency spectrum used by each of the different digital radio standards is shown in Fig. 1. The frequencies supported by the standards range from a few kilohertz to several gigahertz, but the actual frequencies used for broadcasting are not diverse [4],[5]. Therefore, the RF Tuner Chip has been implemented in such a way that all of the blocks, with the exception of the Low Noise Amplifier (LNA), support all digital radio broadcasting. In case of the LNA, four different LNAs have been designed for different frequency ranges, and a different LNA is used depending on the digital radio standard selected.

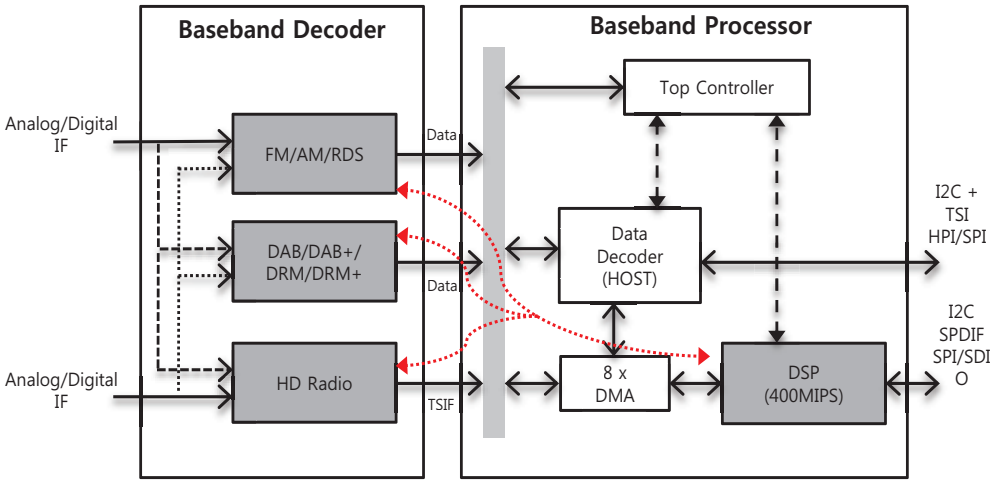

Figure 2: Architecture of the Multi-Standard Digital Radio Chipset.

3 Multi-Standard Digital Radio Chipset

The proposed Multi-Standard Digital Radio Chipset that supports DRM, DRM+, DAB, DAB+, HD Radio has been designed with 65 nm CMOS fabrication technology. Fig. 2 illustrates its high level architecture that takes care of the data decoding for DRM, DRM+, DAB, DAB+, HD Radio. It consists of a Baseband Decoder and Baseband Processor. The Baseband Decoder block extracts the digital data from the RF signal received for each of the different standards. The Baseband Processor controls the Baseband Decoder and extracts the audio signal from the digital data. The Baseband Decoder block consists of 100% hardware logic. The Baseband Processor includes a DSP core which enables software changes and updates.

The internal structure of the Baseband Decoder is shown in Fig. 3. The signal from the RF module is sent to the ADC as input. The input signal is separated into I and Q signals in the Low Pass Filter (LPF) and IQ Mixer block. HD Radio uses its own IQ Decoder and LPF for I/Q signal separation for DAB/DAB+/DRM/DRM+. The I/Q signals separated are sent to the Time Filter and Post Auto Gain Controller (AGC) block, respectively. The compensated I/Q signal is changed from frequency domain data to time domain data through the FFT block. Unlike other digital radio signals, DAB and DAB+ use null packets for frame synchronization in the received signal. Therefore, the Null Detector is only used for DAB/DAB+ reception. The FFT, Timer Filter, and Post AGC blocks are used for processing all digital radio standards [9]. The Equalizer, Time Interleaver, and Viterbi Decoder blocks are also used commonly for decoding all digital radio standards signals.

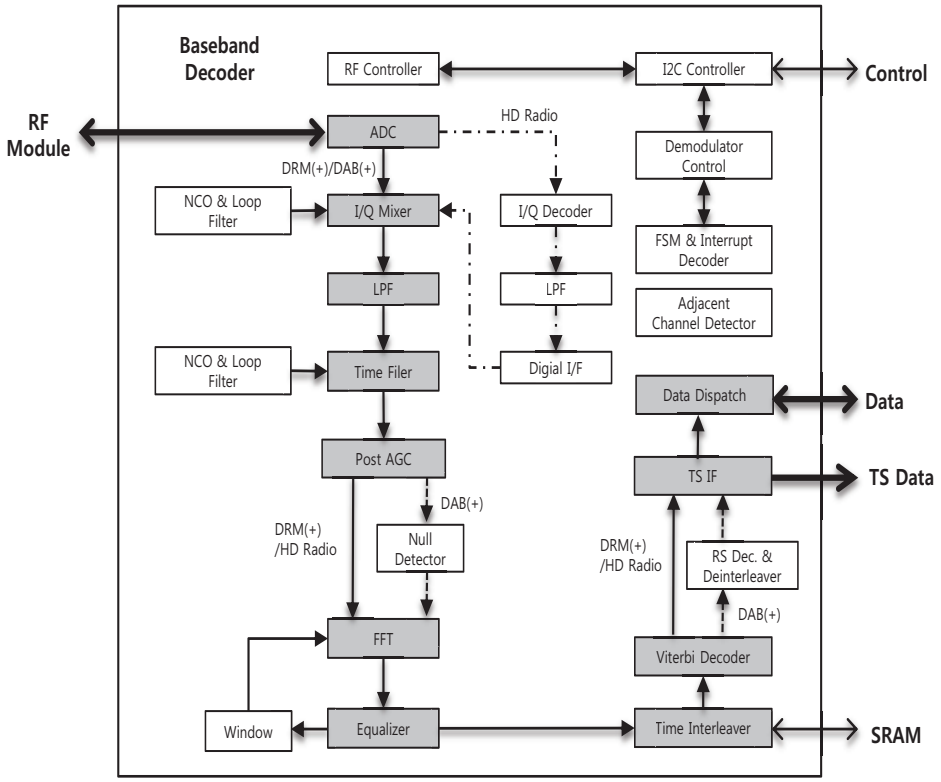

Figure 3: Internal structure of the Baseband Decoder.

The decoded signal is sent to the Baseband Processor either through the TS interface or Data Dispatch blocks, depending on the data type. The use of the standard-specific or common blocks is set by control signals sent through the I2C interface. Table 2 shows the percentage of logic usage of the different blocks that consist the Baseband Decoder when decoding each digital radio standard signal. D-AGC and D-Mixer have been implemented to be 100% applied in all standards. The other internal blocks have been designed to share over 50% of the logic in order to minimize the percentage of unused logic when decoding a particular digital radio standard. All of the implemented internal blocks are designed to decode DAB and DAB+ as a basis. Therefore, decoding DAB and DAB+ use 88% of the logic.

As shown in Fig. 4, the Baseband Processor controls the Baseband Decoder and executes part of the digital radio standard signal processing. The DSP Core operates at 180 MHz, performs 24-bit computation, and executes at 400 MIPS. The DSP Core uses TS interface and DRAM-like interface with the Baseband Decoder to receive data. It is connected directly through the AHB bus. The control signals for the Baseband Decoder are exchanged through the

Table 2: Logic usage of the Baseband Decoder

Module	DAB/DAB+	DRM/DRM+	HD Radio
D-Mixer	100%	100%	100%
STR Loop	80%	80%	80%
CR Loop	80%	80%	80%
D-AGC	100%	100%	100%
FFT	100%	50%	100%
Equalizer	100%	80%	70%
Diversity	100%	90%	90%
Demapper	100%	80%	90%
Deinterleaver	80%	80%	80%
Viterbi	80%	80%	80%
RS	100%	100%	100%
FSM	30%	30%	30%
Average	88%	86%	86%

I2C interface. In other to ease the integration with diverse systems, SPI, TS, and SPDIF interfaces are also supported.

In Fig. 5, the overall architecture of the RF Tuner chip capable of receiving diverse frequency bands used in worldwide radio standards is shown. The RF Tuner chip consists of RF Front-end, Analog IF Signal Processor, Frequency Synthesize, Digital and Analog Interface blocks. The RF Front-end block consists of an LNA and Mixer. There are four LNAs corresponding to different frequency bands. The Mixer performs down conversion of the signal from the desired frequency band into low frequency bands [10]-[12].

In order to enable backwards compatibility with DRM, DRM+, DAB, DAB+, HD Radio standards based digital radio, the RF Chipset implemented in this paper was implemented with the ability to receive analog AM and FM radio. The RF implements 4 LNAs in order to amplify the signal from different frequency bands ranging from a few kilohertz to 1.6 GHz. Digital signal is processed in the IF band in order to eliminate noise and distortion in the analog signal [10]. To enable reception of analog signals from different frequency bands, the RF front-end noise figure was designed with target performance of under 4 dB. A 1 dB margin was added taking into account performance degradation during chip fabrication. The design margin for P1dB and IIP3, which represent the RF Tuner chip's gain and linearity performance, was also secured.

4 Implementation Results

Fig. 6 shows the BER measurements of the implemented Baseband Demodulator chip for digital radio. The BER measurements show the decoding perfor-

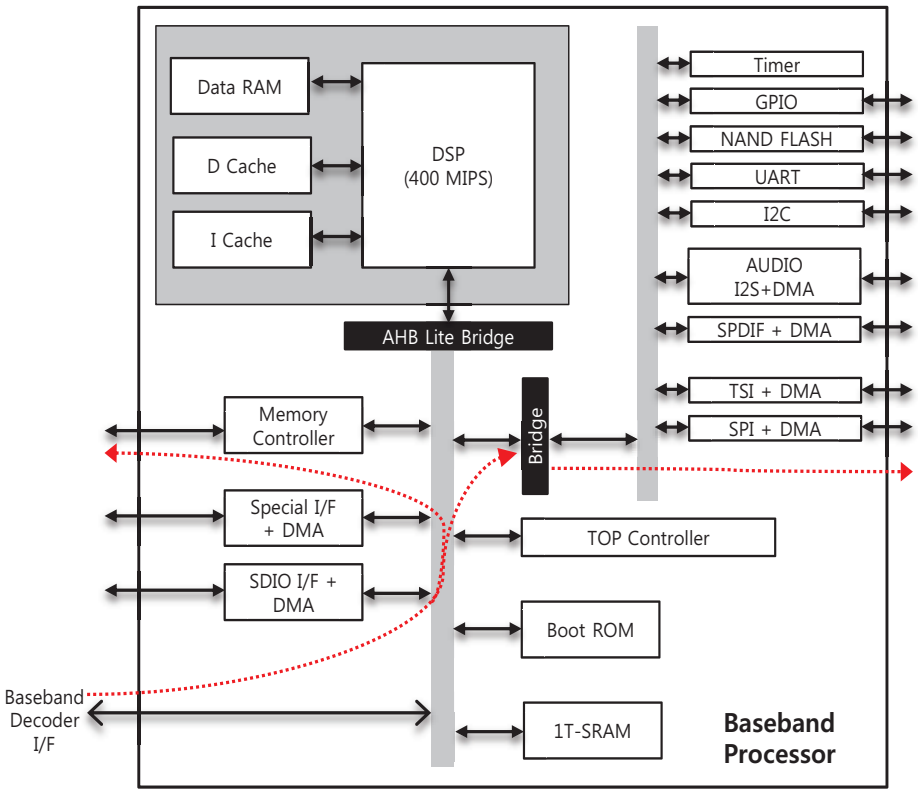

Figure 4: Internal structure of the Baseband Processor.

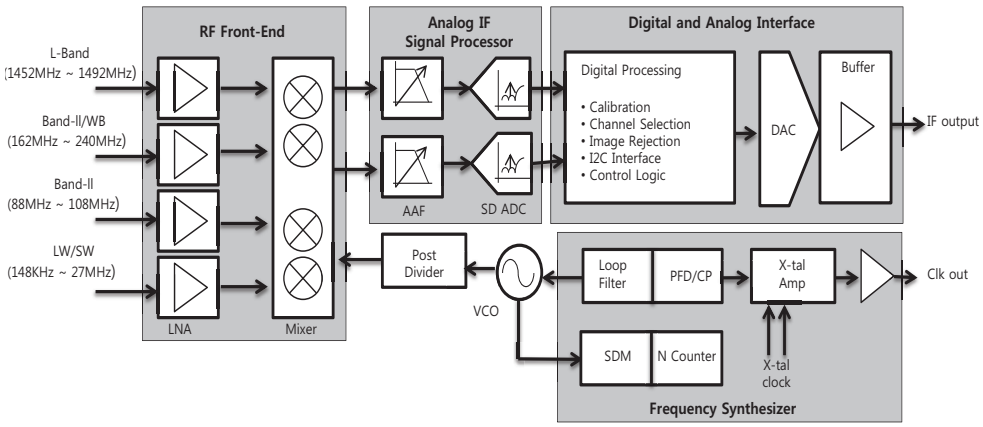

Figure 5: Architecture of the RF Tuner chip.

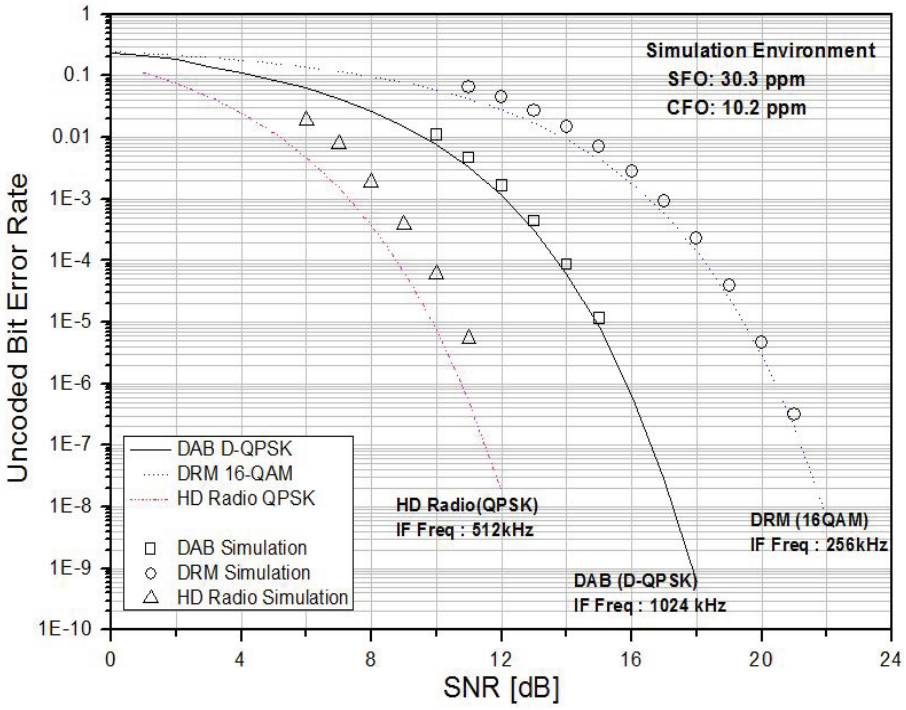

Figure 6: BER performance of the Baseband Demodulator.

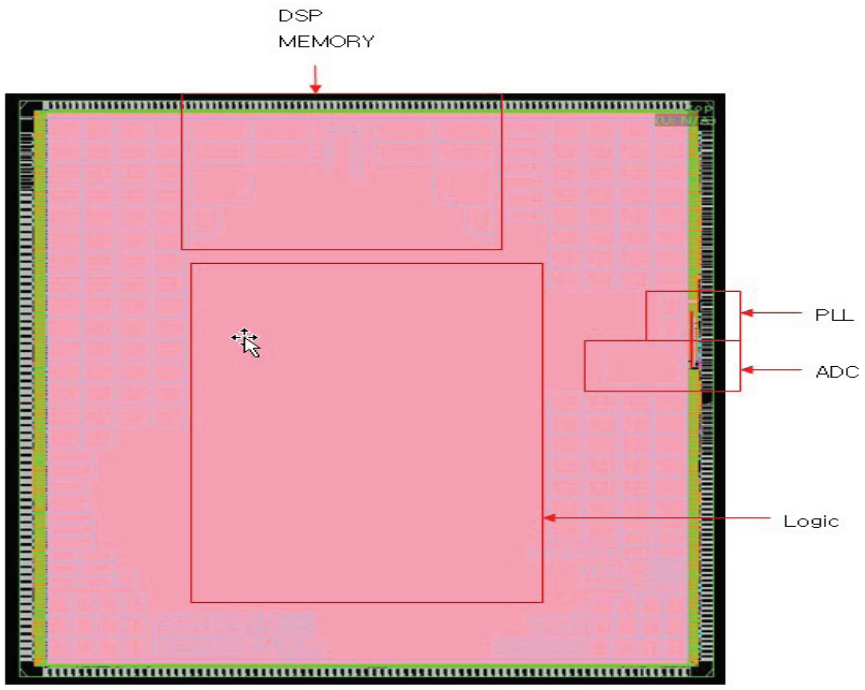

Figure 7: Chip layout of the Baseband Demodulator.

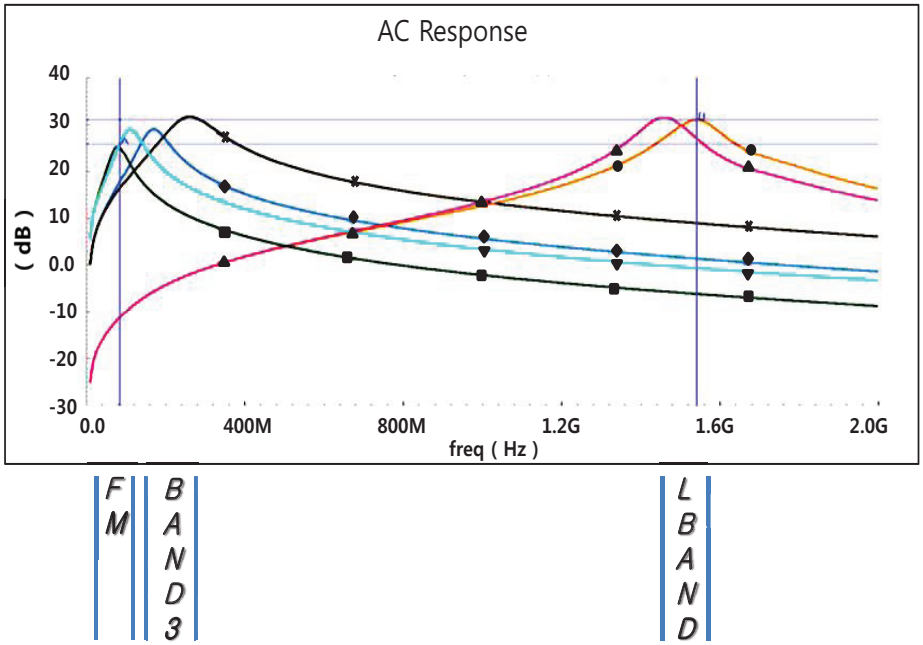

Figure 8: Front-end performance of the RF Tuner chip.

Table 3: Measurement performance of the RF Tuner chip

	Target	AM	FM	Band-III	L-Band
NF	$<$ 4dB	-	2.58dB	2.24dB	2.8dB
Gain	$>$ 25dB	11dB	25.7dB	29dB	31dB
PldB	-	-10.5dBm	-11.5dBm	-19.2dBm	-22.9dBm
IIP3	-	-2dBm	-9dBm	-10dBm	-15.5dBm
Sll	$<$ -5dB	-6dB	-15dB	-7.2dB	-6.18dB

mance of the Baseband Demodulator chip. The C/N ratio measured was 6.9 dB when receiving DAB/DAB+ and 20.1 dB when receiving DRM/DRM+. In Fig. 7, the chip layout of the Baseband Demodulator is shown. Approximately 50% of the total Demodulator dimension consists of the Baseband Decoder logic. The remaining area consists of the DSP Core and SDRAM which is used for computation. In order to implement a single chip with the RF Tuner chip, 65 nm CMOS process was used. The die size of the Baseband Demodulator chip is 6.5 mm x 6.5 mm.

In Fig. 8, the simulation results of the RF front-end block for each frequency band are shown. Over 10 to 30 dB amplification can be seen for each frequency band. Table 3 shows the target design performance of the implemented RF Tuner chip.

5 Conclusion

In this paper, implementation of a Baseband Demodulator and RF Tuner chips for reception of DAB/DAB+, DRM30/DRM+, and HD Radio digital radio standards is presented. The internal blocks of the Baseband Demodulator chip is designed to receive all digital radio broadcasts. When receiving and processing a particular digital radio broadcast, the unused logic consists less than 14% which shows the efficiency of the logic design. The use of DSP Core provides flexibility in the implementation, enabling it to deal with possible future changes in the standards. The RF Tuner chip uses 4 LNAs and performs performance compensation in the digital domain. This design resulted in high performance in all frequency bands tested. The RF Tuner and Baseband Demodulator chips implemented in this paper enable the design of a single chip implementation for reception of digital radio broadcasts worldwide. The chips use the same CMOS fabrication technology in order to facilitate the integration of the two chips into one in the future.

ACKNOWLEDGEMENTS. This research was supported by the IT R&D program of MSIP/KEIT [10039196, Smart Platform Development for Integrating Worldwide Radio Technology to Smart Devices].

References

[1] W. Hoeg and T. Lauterbach. 2009. Digital Audio Broadcasting: Principles and Applications of DAB, DAB + and DMB, John Wiely & Sons.

[2] G. Kalivas. 2009. Digital Radio System Design , John Wiely & Sons.

[3] C. Gandy. 2003. DAB: an introduction to the Eureka DAB System and a guide to how it works, BBC R&D White Paper.

[4] ETSI. 2006. Radio Broadcasting Systems; Digital Audio Broadcasting (DAB) to mobile, portable and fixed receivers, ETSI EN 300 401, V1.4.1.

[5] ETSI. 2009. Digital Radio Mondiale (DRM); System Specification, ETSI ES 201 980, V3.1.1.

[6] Kyung-Won Park, Seong-Jun Kim and Kyung-Taek Lee. 2013. Transmission Rate Enhancement Schemes for Digital Radio Mondiale Systems, *International Journal of Multimedia and Ubiquitous Engineering*, Vol.8, No.1, 225-234.

[7] R. Struble, J. D'Angelo, J. McGannon, D. Salemi. 2006. AM & FM's digital conversion: how HD radio TM will spur innovative telematics services

for the automotive industry, *IEEE Vehicular Technology Magazine*, Vol.1, Issue.1, 18-22.

[8] Myung-Sun Baek, Yong-Hoon Lee, Sora Park, Geon Kim, Bo-mi Lim, and Yong-Tae Lee. 2013. Field Trials and Evaluations of In-Band Digital Radio Technologies: HD Radio and DRM+, *IEEE Trans. Broadcasting*, Vol.59, Issue.3, 401-411.

[9] Young-Hwan You and Kyung-Taek Lee. 2010. Accurate Pilot-Aided Sampling Frequency Offset Estimation Scheme for DRM Broadcasting Systems, *IEEE Trans. Consumer Electronics*, Vol.56, No.4, 558-563.

[10] Seong-Jun Kim, Kyung-Won Park, Kyung-Taek Lee, and Hyung-Jin Choi. 2012. Digital Tuner Implementation Using FM Tuner for DRM Plus Receivers, *IEEE Trans. Consumer Electronics*, Vol.58, No.2, 311-317.

[11] K. P. Wang, Z. G. Wang, X. M. Lei, J. Z. Zhou, X. Cao, and W. R. Zhang. 2009. Digital Tuner Implementation Using FM Tuner for DRM Plus Receivers, *IEEE International Conference of Electron Devices and Solid-State Circuits*, 39-43.

[12] L. Xuemei, W. Zhigong, and W. Keping. 2011. A design of the frequency synthesizer for DRM/DAB/AM/FM application in 0.18 μm RF CMOS process, *IEEE International Conference of Electron Devices and Solid-State Circuits*, 1-2.